SPI 2017

21st IEEE WORKSHOP ON
SIGNAL AND POWER INTEGRITY

POLITECNICO DI TORINO

7-10 MAY 2017
LAKE MAGGIORE (BAVENO)
ITALY

FINAL PROGRAM

WELCOME TO SPI2017!

Dear colleagues and friends,

It is my honor to serve as the Chair of the 21st IEEE Workshop on Signal and Power Integrity (SPI2017), Lake Maggiore, Italy. On behalf of the organizing committee, I welcome you all to the picturesque small town of Baveno.

Over the past twenty years, the IEEE Workshop on Signal and Power Integrity has evolved into a forum of exchange on the latest research and developments on design, characterization, modeling, simulation and testing for Signal and Power Integrity at chip, package, board and system level. The workshop brings together developers and researchers from industry and academia in order to encourage cooperation.

The SPI2017 technical program includes both oral and poster sessions, one keynote address and one Sunday tutorial. Thanks to the excellent work of the Technical Program Committee headed by the Program Co-Chairs Paolo Manfredi and Igor S. Stievano, we received and selected a very large number of papers, contributing to a very high-level technical program.

This year's edition of SPI will confirm two initiatives that started with SPI2016. First, an Industry Forum will host invited talks from the industry, with the aim of fostering the discussion and cooperation with academia and tool vendors on challenging problems that have no satisfactory solution yet. Second, thanks to our corporate sponsors, a special program for Young Investigators will allow seventeen young scientists to attend SPI and extend their stay for one month, hosted by various research centers in Italy.

As a consolidated tradition, the technical program will be complemented by fascinating social events, allowing the attendees to enjoy the architectural and cultural heritage as well as the relaxing atmosphere of Lake Maggiore and its islands. Two social events have been organized: a welcome reception on May 7th, in the beautiful garden of the conference Hotel facing the lake, and a gala dinner on May 9th, on the nice "Isola Bella", one of the picturesque islands of Lake Maggiore. We are confident that these events will foster discussions and interaction between delegates, in a relaxed and informal atmosphere.

I am very grateful to the many corporate and industry sponsors that supported SPI2017, as well as to my own University, Politecnico di Torino: their generous contribution led to a very successful event. A special thank also to Manuela Trinchero, who supported this event by providing conference secretariat and logistic services at the highest standards and with exceptional dedication.

I wish all of you a very successful conference!

Stefano Grivet-Talocia
SPI2017 General Chair

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Sunday 7 May 2017
14:00-17:30

Substrate Integrated Waveguide (SIW) Technology

Prof. Maurizio Bozzi *(University of Pavia, Italy)*

The advent of the fifth generation of mobile networks (5G) and of the Internet of Things (IoT) is bound to change the scenario of wireless components and systems. The new applications in the microwave and millimeter-wave frequency range requires the implementation of a novel class of circuits, able to integrate data transmission, wireless power transfer, and sensing capabilities in a single wireless device. Among the available implementation technologies, the substrate integrated waveguide (SIW) plays a key role.
The SIW is an integrated version of the classical metallic rectangular waveguide. It is based on a dielectric substrate laminated with metal layers at both faces, where metal vias define the side walls of the waveguide. The major advantages of the SIW technology are the easy design and manufacturing, the low losses, and the complete shielding. In addition, SIW structures can be conveniently integrated with classical planar technologies (e.g., microstrip lines and coplanar waveguides), as well as with active devices and microwave monolithically integrated circuits (MMICs). The SIW technology allows to implement a variety of passive components, active subsystems, and antennas in a simple and cost-effective way, and to integrate entire systems in a single dielectric substrate, thus avoiding complex transitions and undesired parasitic effects.

Part 1: Operation principles and basic structures

In the **first part** of the Tutorial, the basic concepts of the SIW structure will be presented, along with the operation principles and the different mechanisms of loss.
The presentation will cover the different solutions adopted to reduce the size and increase the bandwidth of SIW structures, ranging from slab and ridge SIW interconnects to folded and half-mode configurations. The major modeling techniques and the derivation of equivalent circuit models for design and sensitivity analysis will be discussed.

Part 2: Overview of SIW Technologies, Materials, Components, and Systems

The **second part** of the Tutorial will cover the implementation of SIW components and antennas with different features and substrate materials. In particular, a variety of novel solutions adopted to in the design of SIW components will be discussed, including compact filters, active antennas, and reconfigurable arrays. Finally, the implementation of SIW structures on different materials will be discussed, including paper for eco-friendly systems, textile for wearable and biomedical applications, and 3D-printing for low-cost and ease manufacturing of fully three-dimensional structures.

Maurizio Bozzi was born in Voghera, Italy, in 1971. He received the Ph.D. degree in electronics and computer science from the University of Pavia, Pavia, Italy, in 2000.

He held research positions with various universities worldwide, including the Technische Universität Darmstadt, Germany; the Universitat de Valencia, Spain; and the École Polytechnique de Montréal, Canada. In 2002, he joined the Department of Electronics, University of Pavia, where he is currently an Associate Professor. He is also a Guest Professor of the Tianjin University (China) for the term 2015-2017.

He has authored or co-authored more than 95 journal papers and 250 conference papers. He co-edited the book *Periodic Structures* (Research Signpost, 2006) and co-authored the book *Microstrip Lines and Slotlines* (Artech House, 2013). His main research interests concern the computational electromagnetics, the substrate integrated waveguide technology, and the use of novel materials and fabrication technologies for microwave circuits (including paper, textile, and 3D printing).

Prof. Bozzi is an Elected Member of the Administrative Committee of the IEEE Microwave Theory and Techniques Society (MTT-S) for term 2017–2019 and a Co-Chair of the Meeting and Symposia Committee of MTT-S AdCom for year 2017. He was the Secretary of IEEE MTT-S for year 2016 and a member of the General Assembly (GA) of the European Microwave Association (EuMA) for the term 2014–2016. He is an associate editor for the IEEE Microwave and Wireless Components Letters, the IET Electronics Letters, and the IET Microwaves, Antennas and Propagation. He is the General Chair of the IEEE MTT-S International Microwave Workshop Series-Advanced Materials and Processes (IMWS-AMP 2017), Pavia, Italy, 2017. He was the General Chair of the IEEE International Conference on Numerical Electromagnetic Modeling and Optimization (NEMO2014), Pavia, Italy, 2014, and the General Chair of the IEEE MTT-S International Microwave Workshop Series on Millimeter Wave Integration Technologies, Sitges, Spain, 2011.

He received several awards, including the 2015 Premium Award for Best Paper in IET Microwaves, Antennas & Propagation, the 2014 Premium Award for the Best Paper in Electronics Letters, the Best Student Paper Award at the 2016 IEEE Topical Conference on Wireless Sensors and Sensor Networks (WiSNet2016), the Best Paper Award at the 15th Mediterranean Microwave Symposium (MMS2015), the Best Student Award at the 4th European Conference on Antennas and Propagation (EuCAP 2010), the Best Young Scientist Paper Award of the XXVII General Assembly of URSI in 2002, and the MECSA Prize of the Italian Conference on Electromagnetics (XIII RiNEm), in 2000.

KEYNOTE

Monday 8 May 2017
08:50-09:40

Signal Integrity Challenges in a "Data Everywhere" World

Howard Heck *(Intel Corporation, USA)*

Data ubiquity is here. Our lives involve nearly constant interaction with digital data, wherever we go, whatever we do. We carry smart phones and laptop PCs with 100s of GB of storage running applications that interact with petabyte capacity data servers all over the globe. In addition, new applications continue to emerge, such as automobiles that are capable of autonomous driving and/or high definition content presentation. These trends lead to a couple of interesting impacts:

1. bandwidth demand is growing by 40% per year (25x-30x over the next decade).
2. data transmission systems are being applied in new environments that can have dramatically different requirements (e.g. power, reliability, environment) than in the past.

From these impacts a variety of signal integrity challenges emerge, including:

- operation in very small, thin form factors which drive crosstalk and radio interference concerns
- battery operation, which demands minimized power during operation and the ability to shut off features when not in use
- development of signaling standards that provide the required performance scaling across a range of interconnect channels without exceeding the power envelope
- exceptionally short design and validation cycles which drive the need to design transceiver that can characterize signaling link robustness

This talk will dwelve into these challenges in detail and offer some thoughts on opportunities for research and innovation in delivering solutions.

Howard Heck is a Principal Engineer at Intel Corporation, where he specializes in Signal Integrity. In his 30 years in the industry He has held various technical and management positions related to computer system design and manufacturing. His most recent responsibilities include the development of specifications and product solutions for Universal Serial Bus 3.0/3.1, spanning from initial spec development to post-silicon validation. In addition to USB, He is currently involved with development of 50Gb/s Ethernet backplane specifications and products. He coauthored *"Advanced Signal Integrity for High-Speed digital Designs"*, a graduate level textbook on Signal Integrity, and from 1998 through 2009 He taught Signal Integrity at the Oregon Graduate Institute. He is the chair for the IEEE Oregon joint CPMT-CAS chapter. He has 25 patents with 21 others pending.

Sunday, 7 May 2017

14:00 - 17:30	**Tutorial** Chair: **S. Grivet-Talocia**
	Substrate Integrated Waveguide (SIW) Technology **M. Bozzi** *(University of Pavia, Italy)*
14:00 - 15:30	**Part 1: Operation principles and basic structures**
15:30 - 16:00	Coffee break
16:00 - 17:30	**Part 2: Case Study in Designing for Power Integrity**
18:30	Welcome reception

Monday, 8 May 2017

08:00 Registration opens

08:30 - 08:50 Opening Ceremony
Chair: **S. Grivet-Talocia**

08:50 - 09:40 Keynote
Chair: **S. Grivet-Talocia**

Signal Integrity Challenges in a "Data Everywhere" World
Howard Heck (*Intel Corporation*)

09:40 - 10:40 Session 1: **Noise Analysis & Reduction Techniques**
Chair: **J. Shutt-Ainé**

A Multilayer Removable EBG Based Common Mode Filter for High Speed Buses
C. Olivieri [(1)], F. de Paulis [(1)], A. Orlandi [(1)], S. Connor [(2)], P. Dixon [(3)], M. Korrami [(3)]
[(1)] *University of L'Aquila, Italy;* [(2)] *IBM, USA;* [(3)] *LAIRD Technologies, USA*

Efficient Design of Continuous Time Linear Equalization for Loss Dominated Digital Links (STUDENT PAPER)
T. Reuschel, J.B. Preibisch, C. Schuster
Hamburg University of Technology (TUHH), Germany

A Perturbative Approach to Predict Eye Diagram Degradation in Differential Interconnects Subject to Asymmetry and Nonuniformity
P. Manfredi [(1)], X. Wu [(2)], **F. Grassi** [(2)], D. Vande Ginste [(1)], S. A. Pignari [(2)]
[(1)] *Ghent University, Belgium;* [(2)] *Politecnico di Milano, Italy*

10:40 - 11:10 Coffee break

10:40 Exhibition opens

11:10 - 12:30 Session 2: **Stochastic Analysis & Uncertainty Quantification**
Chair: **Z. Zhang**

Speeding Up Rare Event Simulations Using Kriging Models (STUDENT PAPER)
A. K. Tyagi [(1)], X. Jonssony [(2)], T. G. J. Beelen [(1)], W. H. A. Schilders [(1)]
[(1)] *University of Technology, Eindhoven, NL;* [(2)] *Mentor Graphics, Grenoble, FR*

Time-Domain Variability Analysis of General Linear Systems Terminated with Nonlinear Devices
Y. Ye, D. Spina, P. Manfredi, D. Vande Ginste, T. Dhaene
Ghent University, Belgium

Time-Domain Variability Analysis of Large Circuits with Stochastic Linear Terminations
Y. Tao [(1)], K. Guo [(1)], **F. Ferranti** [(2)], B. Nouri [(1)], M. Nakhla [(1)], R. Achar [(1)]
[(1)] *Carleton University, Ottawa, Canada;* [(2)] *IMT Atlantique, CNRS Lab-STICC, Brest, France*

Monte Carlo Estimation of Sparse Grid Interpolation Residual for Stochastic Collocation of High-Order Systems with Uncertainties (STUDENT PAPER)
X. Chen, X. Ma, A. Rong, J.E. Schutt-Ainé, A.C. Cangellaris
University of Illinois at Urbana-Champaign, USA

12:30 - 14:00 Lunch break

14:00 - 15:00 Session 3: **Electromagnetic Modeling**
Chair: **D. Vande Ginste**

Accurate Characterization of Coaxial Transmission Line via Higher Order Moment Method Solution of Novel Single-Source Surface Integral Equation
F.S.H. Lori [(1)], M.S. Hosen [(1)], M. Shafieipoury [(2)], A. Menshovz [(3)], **V. Okhmatovski** [(1)]
[(1)] *University of Manitoba, Canada,* [(2)] *Manitoba HVDC Research Centre, Canada,* [(3)] *The University of Texas at Austin, USA*

A Magneto-Quasi-Static Surface Formulation to Calculate the Impedance of 3D Interconnects with Arbitrary Cross-section (STUDENT PAPER)
U.R. Patel, S.V. Hum, P. Triverio
University of Toronto, Toronto, Canada

Parameter Optimization for Rise Time of Subnanosecond Pulser Based on Avalanche Transistors
M.-X. Gao, Y.-Z. Xie, Y.-H. Hu
Xi'an Jiaotong University, China

15:00 - 17:30 **Poster session** (includes coffee break)
Chair: **I.S. Stievano, P. Manfredi**

P-04 ***Simultaneous Switching Noise Modelling and Characterization in Production Environments***
J. Yan, Y. Tretiakov, H. Lan
Rambus Inc., Sunnyvale, CA, USA

P-10 ***Crosstalk and Field Analysis of Arc shape Coaxial Via for High Speed Digital Signals***
S. Theepak, Nandakumar C M, B. Devadas, R. Selva Priya, Gauraw Srivastava
Centre for Development of Telematics, Bangalore, India

P-12 ***Design of High Speed Physical Layer Interconnects through System Modeling, Simulation and Correlation***
A. Anil Kumar
Segate Technology HDD, India

P-19 ***Crosstalk Simulation of Multiple Insulated Twisted Pairs based on Transmission Line Theory***
F. Distler, G. Gold, K. Thurn, J. Schür, M. Vossiek
Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany

P-20 ***A Comparison of Typical Surface Finishes on the High Frequency Performances of Transmission Lines in PCBs***
B. Curran, I. Ndip, K.-D. Lang
Fraunhofer Institute of Reliability and Microintegration, Germany

P-28 ***FFT-Based Macromodeling of Power Delivery Network with Uncertainties Using Latency Insertion Method*** (STUDENT PAPER)
R.F. Kummerer, X. Chen, J.E. Schutt-Ainé, A.C. Cangellaris
University of Illinois at Urbana-Champaign, USA

P-34 ***Analysis of Pin-To-Capacitor Spacing in Power Delivery Networks Designed as Parallel-Plate Power-Ground Pairs***
I. Erdin [1], R. Achar [2]
[1] Engineering Design Services Celestica Inc., Canada; [2] Carleton University, Canada

P-35 ***Uncertainty Analysis of Arbitrary Probability Distribution Based on Stieltjes Process***
G. Zhang, J. Bai, L. Wang, X. Peng
Harbin Institute of Technology, China

P-39 ***Impact of Flexible PCB on DDR4 Channel Memory Performance***
K. Krohne [1], H. Fahmy [2], H. Oie [2], F. Elsisy [2], D. Di Febo [3]
[1] CST AG; [2] Intelligent Solutions BVBA, Belgium; [3] CST Italy

P-50 ***The Estimation of EMI-induced Phase Noise and Jitter on Oscillator/Clock Signals***
M. Mehri, S. Heidari, and N. Masoumi
University of Tehran, Tehran, Iran

P-51 ***Minimizing Core Supply Noise in a Power Delivery Network by Optimization of Decoupling Capacitors using Simulated Annealing***
J.N. Tripathi [1], P. Damle [2], R. Malik [1]
[1] STMicroelectronics Pvt. Ltd., India; [2] Texas Instruments, India

P-53 ***Feasibility of Single Wire Communication for PCB-level Interconnects***
S. Kotethota [1], G. Hada [2], P. Ramaswamy [2], Dipanjan Gope [1]
[1] Indian Institute of Science, Bangalore, India; [2] Intel Corporation, Bangalore, India

P-54 ***Statistical Prediction of Planar Power Consumption Distribution in Digital System Layout/PCB***
S. Heidari, M. Mehri, N. Masoumi
University of Tehran, Tehran, Iran

P-55 ***Simple Approach for brief RF Characterization of thin 3D printable Dielectrics***
M. Sippel, K. Lomakin, G. Gold, T. Reitberger, S. Neermann, K. Helmreich
Friedrich-Alexander University Erlangen-Nuremberg, Germany

P-58 ***Electrical Performance of Carbon-Based Power Distribution Networks with Thermal Effects***
A. Magnani [1], M. de Magistris [1], S. Heidari [2], A. Todri-Sanial [3], A. Maffucci [4]
[1] University Federico II, Naples, Italy; [2] University of Tehran, Iran; [3] University of Montpellier, France; [4] University of Cassino and Southern Lazio, Italy

P-61 ***Causal Transmission Line Model Incorporating Frequency-Dependent Linear Resistors*** (STUDENT PAPER)
A. Takeshige, Y. Ito, K. Takano, K. Katayama, T. Yoshida, M. Fujishima, S. Amakawa
Hiroshima University, Japan

P-70 ***Fusion of First-Principles and Statistical Analyses in Complex Electronics Systems***
S. Lin [1], Z. Peng [1], T. Antonsen [2]
[1] University of New Mexico, USA; [2] University of Maryland, USA

P-71 ***Air-Filled Substrate Integrated Waveguide: a Low Cost Self-Packadged Technological Platform For High Performance Millimeter-Wave Circuits***
A. Ghiotto
Univ. Bordeaux, France

17:30 Exhibition closes

18:30 Free dinner

Tuesday, 10 May 2016

08:00 Registration opens

08:30 Exhibition opens

08:30 - 09:30 Session 4: **Measurements & Characterization**

Chair: **U. Arz**

Characterization Techniques of a Terabit Backplane using New Figures of Merit

M. Resso

Keysight Technologies, Santa Rosa, CA, USA

Measurement Based VRM Modeling

S.M. Sandler (**H. Barnes**)

PICOTEST, Phoenix, AZ, USA

Effective Method to Characterize the Bandwidth of Unknown Receiver

J. Liao, C. Mason, S. Christianson

Intel Corporation, Hillsboro, Oregon, USA

09:30 - 10:30 Session 5: **Power Delivery Networks**

Chair: **G. Signorini**

Mesh-Sensitivity based Decoupling Capacitor Sizing and Placement for Power Delivery Networks (STUDENT PAPER)

N. Ambasana, D. Gope

Indian Institute of Science, Bangalore, India

Power delivery network impedance characterization for high speed I/O interfaces using PRBS transmissions

D.M. Garcia-Mora (1), J. Garcia-Huanaco (1), V.J. Zuniga-Marquez (1), C.J. Franco-Tinoco (1), F. Yahyaei-Moayyed (2), Kyle S. Unger (2)

(1) Intel Guadalajara Design Center, Mexico; (2) Intel Corporation, AZ, USA

Thermal Aware IR drop using Mesh Conforming Electro-Thermal Co-Analysis

J. Sercu, **H. Barnes**

Keysight Technologies, Belgium

10:30 - 11:00 Coffee break

11:00 - 12:20 Session 6: **Macromodeling & MOR**

Chair: **M. Nakhla**

Order Reduction of Volterra and Volterra-Laguerre Models

M. Telescu, N. Tanguy

Université de Bretagne Occidentale (UBO), Brest, France

Rational multi-delay models for long interconnects (STUDENT PAPER)

M. Zyari (1), Y. Rolain (1), F. Ferranti (2)

(1) Vrije Universiteit, Belgium, (2) IMT Atlantique, CNRS Lab-STICC, Brest, France

A Novel Parametric Macromodeling Technique for Electromagnetic Structures with Propagation Delays (STUDENT PAPER)

M. Sgueglia (1), A. Sorrentino (1), M. de Magistris (1), D. Spina (2), D. Deschrijver (2), T. Dhaene (2)

(1) University Federico II, Naples, Italy; (2) Ghent University, Belgium

Simulation of Buck Converters via Numerical Inverse Laplace Transform

R. Trinchero, I.S. Stievano, F.G. Canavero

Politecnico di Torino, Italy

12:30 - 14:00 Lunch break

14:00 - 15:20 Session 7: **High-Speed Link Design and Modeling**

Chair: **M. Telescu**

SI Analysis of DDR Bus during Read/Write operation transitions

N. Bhagwath (1), A. Muranyi (1), D. Smirnov (1), C. Ferry (1), A. Sato (2), M. Ono (2), S. Ikeda (2), Y. Sugaya (2), T. Fukuhara (2), R. Wolff (3)

(1) Mentor Graphics, USA; (2) Socionext, Japan, (3) Micron, USA

Deep Dive into DDR3 Interface Jitter Contributors

S. SM, K. Scholz, T. Bandyopadhyay, S. Moharil, S. Sinha, R. DeMoor

Texas Instruments Inc., Dallas, TX, USA

Exploration of Differential Via Stub Effect Mitigation by Using PAM4 and PAM8 Line Coding (STUDENT PAPER)

K. Scharff (1), T. Reuschel (1), X. Duany (2), H.-D. Bruns (1), C. Schuster (1)

(1) Hamburg University of Technology (TUHH), Germany; (2) IBM Research and Development, Germany

A 45-GHz Wireless Transmission for a Wireless Interconnect Network-on-Board

T. Le Gouguec, P.-M. Martin

Université de Bretagne Occidentale (UBO), Brest, France

15:30 - 16:00 Coffee break

Tuesday, 10 May 2016

16:00 - 17:30 **Industry Forum and Panel Discussion**
Chair: **R. Achar, S. Grivet-Talocia**

William J. Lambert
Intel, USA

Hubert Harrer
IBM, Germany

Yutaka Uematsu
Hitachi, Japan

Vijay Boddu
Intel, USA

17:30 Exhibition closes

18:30 Gala dinner

Wednesday, 10 May 2017

08:30 Registration opens

09:00 - 10:00 Session 8: **Transmission Line Modeling**
Chair: **F. Grassi**

Calculations of Frequency Dependent Transmission Line Model for Coupled Exponential Line
A. Wardzinska, W. Bandurski
Poznan University of Technology, Poland

An Improved Equivalent Circuit Model of Spoof Surface Plasmon Transmission Line
D. Yi, X.-C. Wei
Zhejiang University, Hangzhou, China

Transmission Line Model for Rectangular Waveguides accurately incorporating Loss Effects
K. Lomakin, G. Gold, K. Helmreich
Friedrich-Alexander University Erlangen-Nuremberg, Germany

10:00 - 10:40 Session 9: **TSV & 3DIC**
Chair: **A. Maffucci**

Effect of 3D Stack-Up Integration on Through Silicon Via Characteristics (STUDENT PAPER)
D. Dahl [1], I. Ndip [2], K.-D. Lang [2], C. Schuster [1]
[1] Hamburg University of Technology (TUHH), Germany; [2] Fraunhofer Institute for Reliability and Microintegration (IZM), Germany, and Technical University of Berlin, Germany

3D Interconnect Optimization for Single Channel 100-GBps Transmission in a Photonic Interposer
K. Morot [1], A. Farcy [1], T. Lacrevaz [2], C. Bermond [2], P. Artillan [2], B. Flechet [2], H. Jacquinot [3], P. Scheiblin [3]
[1] STMicroelectronics, France; [2] Université de Savoie Mont-Blanc, France; [3] CEA-LETI, Grenoble, France

10:40 - 11:10 Coffee break

Wednesday, 10 May 2017

11:10 - 12:10 Session 10: **Optical & Nano Interconnects**

Chair: **H. Grabinski**

Plasmonic carbon interconnects to enable the THz technology: properties and limits

A. Paddubskaya [1], M. Shuba [1], S. Maksimenko [1], A. Maffucci [2]

[1] *Belarusian State University, Mink, Belarus;* [2] *University of Cassino and Southern Lazio, Italy*

A Performance Comparison of Integrated Graded Index Y-Branch and MMI-Based Optical Splitters in Thin Glass Sheets for PCB Integration

J.-P. Roth, T. Kuhler, E. Griese

University of Siegen, Germany

Analysis of Optical Directional Couplers in Thin Glass Sheets for PCB Integration

J.H. Stosch, T. Kuhler, E. Griese

University of Siegen, Germany

12:10 - 12:30 Closing ceremony

13:30 - 17:20 **20th European IBIS Summit**

Organized by: IBIS Open Forum

13:30 Sign In, Refreshments

13:45 - 14:00 *Welcome and Introductions*

Michael Schäder

Zuken, Germany

Accurate Macromodels of Output Buffers with Pre-/De-emphasis

Gianni Signorini [1], Claudio Siviero [2], Igor Simone Stievano [2], Stefano Grivet-Talocia [2]

[1] *Intel Corporation, Germany;* [2] *Politecnico di Torino, Italy*

Compact Multivariate Surface Approximations for Power-aware I/O models

Claudio Siviero [1], Stefano Grivet-Talocia [1], Gianni Signorini [2], Igor Simone Stievano [1]

[1] *Politecnico di Torino, Italy;* [2] *Intel Corporaton, Germany*

IBIS Update

Mike LaBonte

SiSoft, USA

[Presented by **Michael Schäder**]

Zuken, Germany

15:30 - 15:45 Coffee break

Interconnect Modeling Using IBIS-ISS and Touchstone

Michael Mirmak

Intel Corporation, USA

[Presented by **Stefan Paret**]

CST AG, Germany

IBIS Extensions for Turn-around Cycle Simulations

Nitin Bhagwath [1], Arpad Muranyi [1], Randy Wolff [2]

[1] *Mentor, A Siemens Business, USA;* [2] *Micron Technology, USA*

16:45 - 17:15 Open Discussion

17:15 - 17:20 Closing Remarks

Michael Schäder

Zuken, Germany

17:20 Meeting Ends

SOCIAL EVENTS

The best networking takes always place in a relaxed and informal atmosphere. For this year's SPI edition, two social events have been organized. We hope to see you there!

SUNDAY 7 MAY 2017
18:30

WELCOME RECEPTION

GRAND HOTEL DINO BAVENO (VB)

SPI2017 delegates will meet before the official start of the conference in the beautiful garden of Grand Hotel Dino, the conference Hotel. Our guests will enjoy a breathtaking view of Lake Maggiore and its islands, while enjoying a rich buffet. An informal occasion to meet friends and colleagues and discuss the latest research results.

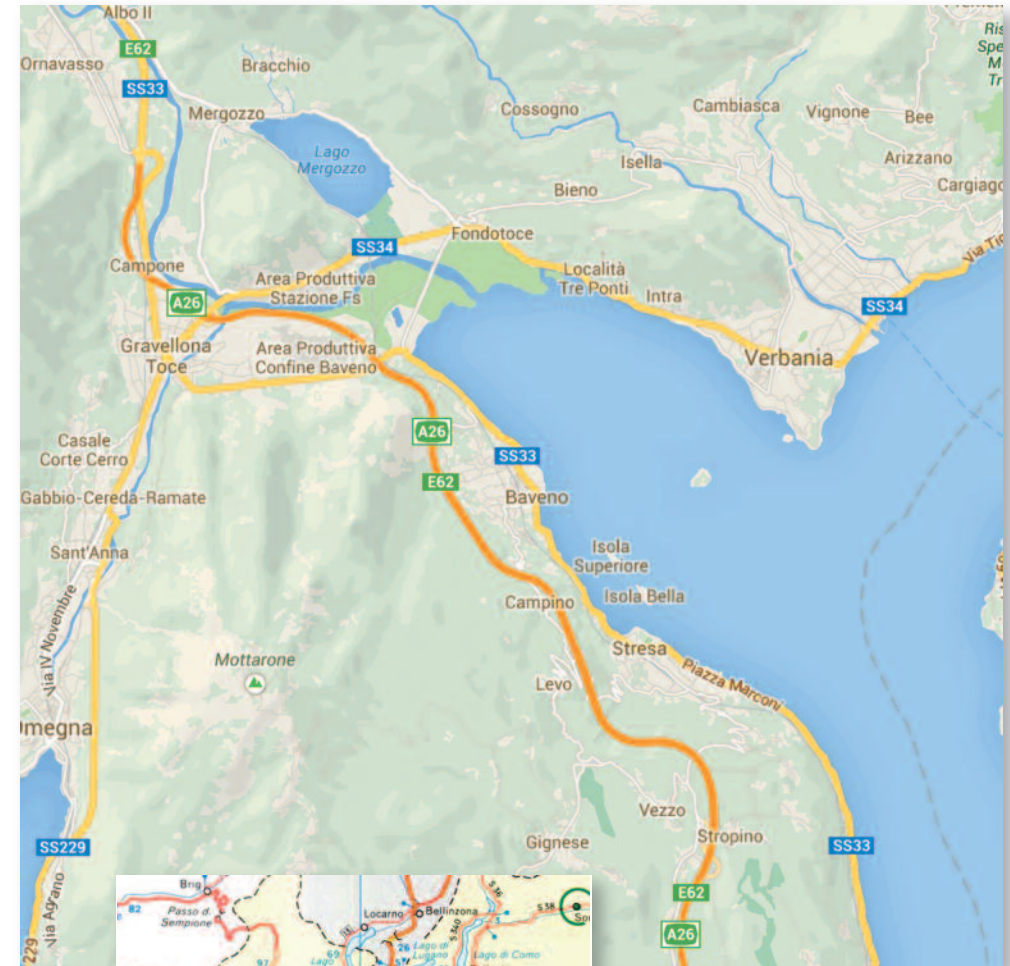
TUESDAY 9 MAY 2017
18:30

GALA DINNER

ISOLA BELLA

The SPI2017 Gala Dinner will take place on the gorgeous “Isola Bella”, the most renowned of the Borromean islands of Lake Maggiore. Delegates will meet at the conference Hotel, where private boats will take them to the island. After a short walk, a welcome cocktail will be offered, followed by a top-class dinner at the Ristorante Elvezia. Situated on a natural stage, Ristolounge Elvezia is an integral part of the Isola Bella. Land of the Borromeo family, the island presents itself to its visitors as a ship sailing the waters of Lake Maggiore, its bow decorated by the Baroque palace and the stern by the magnificent Italian gardens. Plants, flowers, peacocks and sculptures create a spectacular frame for this extraordinary work by mother nature and by man.

VENUE AND MAP



GRAND HOTEL DINO
Corso Garibaldi, 20
28831 Baveno (VB) – Italia
www.dino.zaccherahotels.com

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ACRI Associazione di Fondazioni e di Casse di Risparmio Spa

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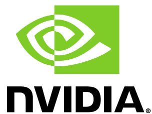

	Sunday May 7	Monday May 7	Tuesday May 9	Wednesday May 10
08:00		08:00 Registration opens 08:30 - 08:50 Opening Ceremony	08:00 Registration opens 08:30 - 09:30 Session 4 **Measurements & Characterization**	08:30 Registration opens
09:00		08:50 - 09:40 Keynote 09:40 - 10:40 Session 1 **Noise Analysis & Reduction Techniques**	09:30 - 10:30 Session 5 **Power Delivery Networks**	09:00 - 10:00 Session 8 **Transmission Line Modeling**
10:00		10:40 - 11:10 Coffee break	10:30 - 11:00 Coffee break	10:00 - 10:40 Session 9 **TSV & 3DIC** 10:40 - 11:10 Coffee break
11:00		11:10 - 12:30 Session 2 **Stochastic Analysis & Uncertainty Quantification**	11:00 - 12:20 Session 6 **Macromodeling & MOR**	11:10 - 12:10 Session 10 **Optical & Nano Interconnects**
12:00		12:30 - 14:00 Lunch break	12:30 - 14:00 Lunch break	12:10 - 12:30 Closing ceremony
13:00				13:30 - 17:20 **IBIS Summit**
14:00	14:00 - 15:30 Tutorial **Substrate Integrated Waveguide (SIW) Technology** – Part I	14:00 - 15:00 Session 3 **Electromagnetic Modeling**	14:00 - 15:20 Session 7 **High-Speed Link Design and Modeling**	
15:00	15:30 - 16:00 Coffee break	15:00 - 17:30 **Poster session** (includes coffee break)	15:30 - 16:00 Coffee break	
16:00	16:00 - 17:30 Tutorial **Substrate Integrated Waveguide (SIW) Technology** – Part II		16:00 - 17:30 **Industry Forum and Panel Discussion**	
17:00				
18:00	Welcome reception	Free dinner	Gala Dinner	
19:00				
20:00				
21:00				
22:00				

SELENE
Eventi e Congressi