

# SPI 2017

21<sup>st</sup> IEEE WORKSHOP ON  
SIGNAL AND POWER INTEGRITY

## CALL FOR PAPERS

7-10 MAY 2017, LAKE MAGGIORE (BAVENO), ITALY

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### CALL FOR PAPERS

Over the past twenty years, the IEEE Workshop on Signal and Power Integrity has evolved into a forum of exchange on the latest research and developments on design, characterization, modeling, simulation and testing for Signal and Power Integrity at chip, package, board and system level. The workshop brings together developers and researchers from industry and academia in order to encourage cooperation.

In view of last year's success, the Committee is looking forward to the 21st Edition which will convene in the charming Northern Lakes region, Italy. The SPI 2017 technical program will include both oral and poster sessions. A number of prominent experts will be giving tutorials on areas of emerging interest. The Conference Proceedings will be published with an ISBN code and will appear in IEEEExplore.

### Topics of Interest

- Modeling and simulation for SI/PI
- Coupled Signal and Power Integrity analysis
- Noise reduction and equalization techniques
- High-speed link design and modeling
- Power distribution networks
- RF/microwave/mixed signal systems
- 3D IC and packages (TSV/SiP/SoC)
- Nano-interconnects and nano-structures
- Electromagnetic theory and modeling
- Transmission line theory and modeling
- Macromodeling, reduced order models
- Electromagnetic compatibility
- Design methodology/flow
- Measurements
- Jitter and noise modeling
- Stochastic/sensitivity analysis
- Electro-thermal modeling
- Chip-package co-design
- Novel CAD concepts
- Optical interconnects

www.spi2017.org



### Important Dates

Paper submission (2-4 pages):  
**January 29, 2017**

Notification of acceptance:  
**February 26, 2017**



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